

Figure 1
Prior Art

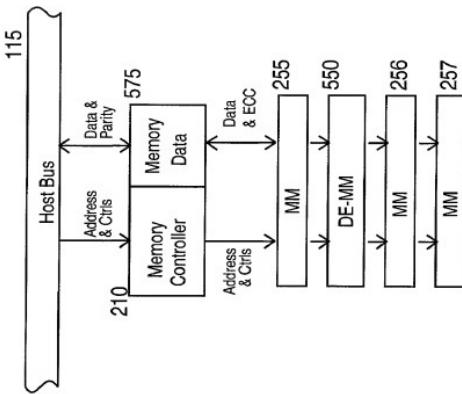


Figure 2a

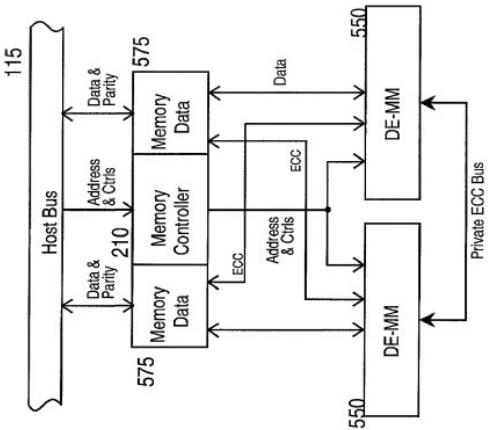


Figure 2b

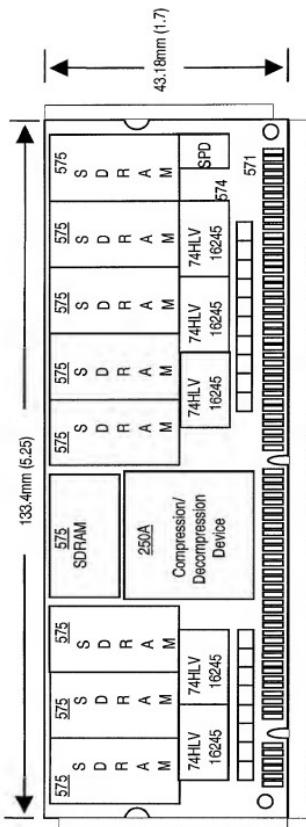


Figure 3a

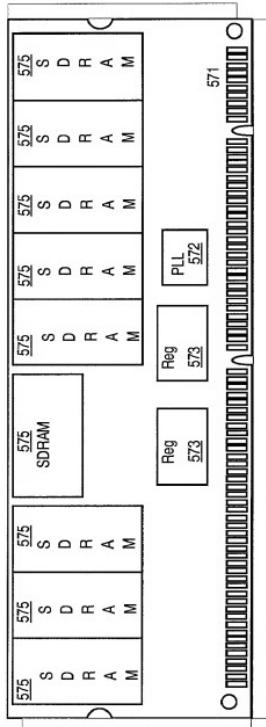


Figure 3b

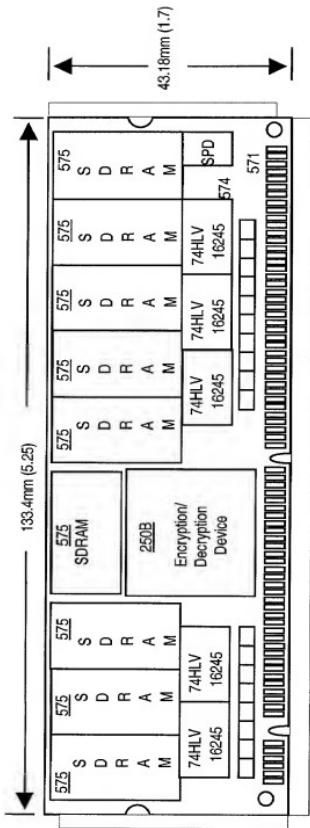


Figure 4a

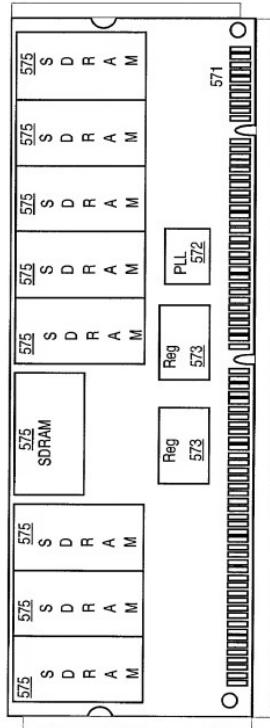


Figure 4b

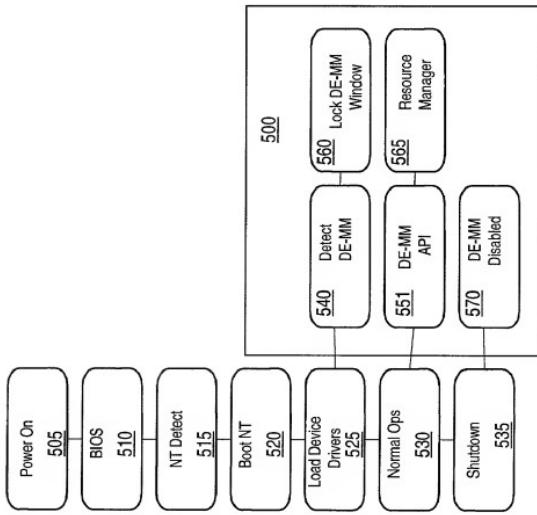


Figure 5

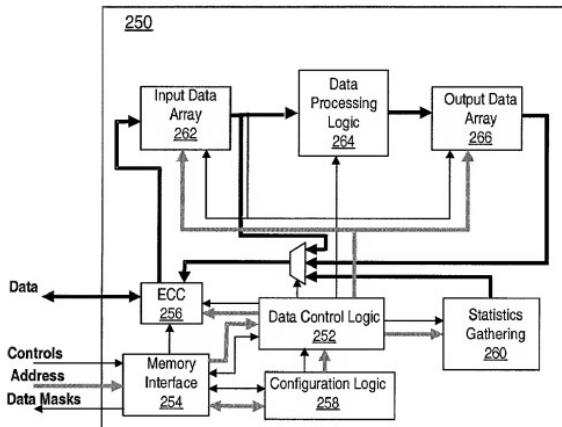


Figure 6
DE-MM device logic

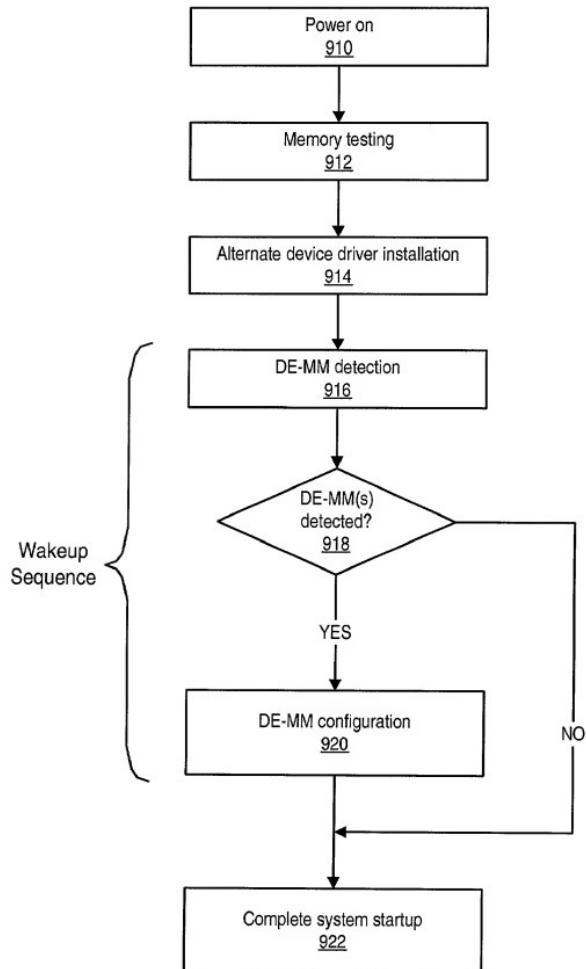


Figure 7a

092407244.042301

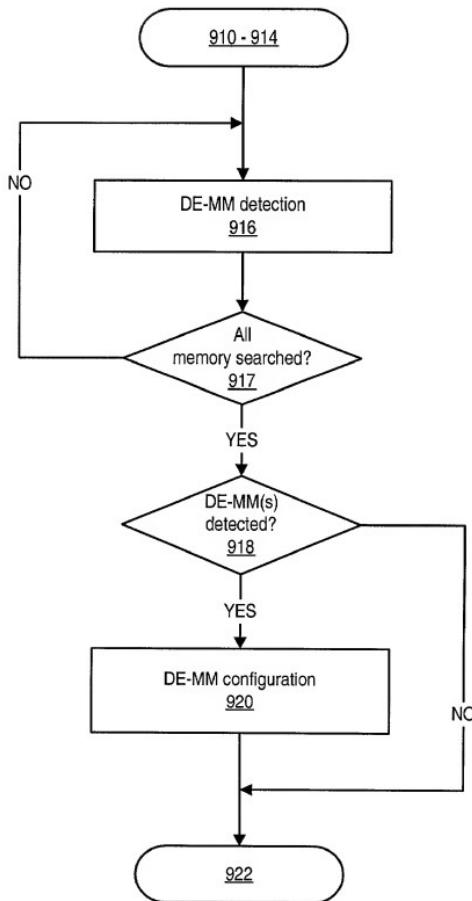


Figure 7b

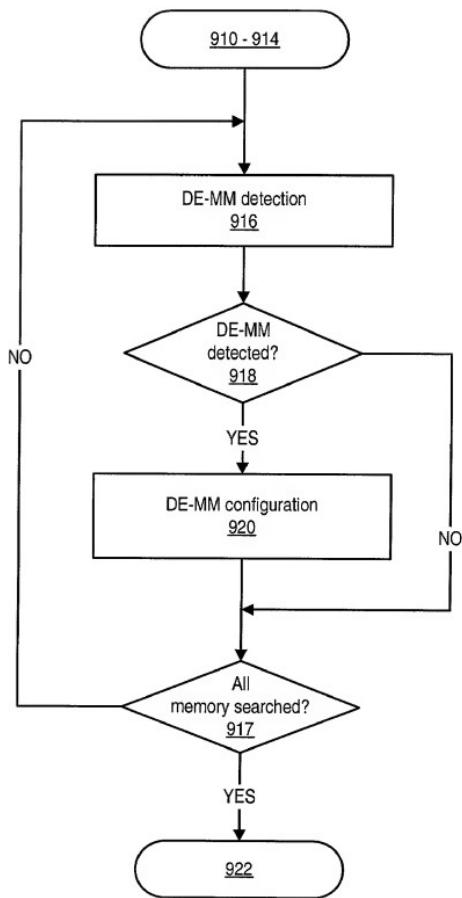


Figure 7c

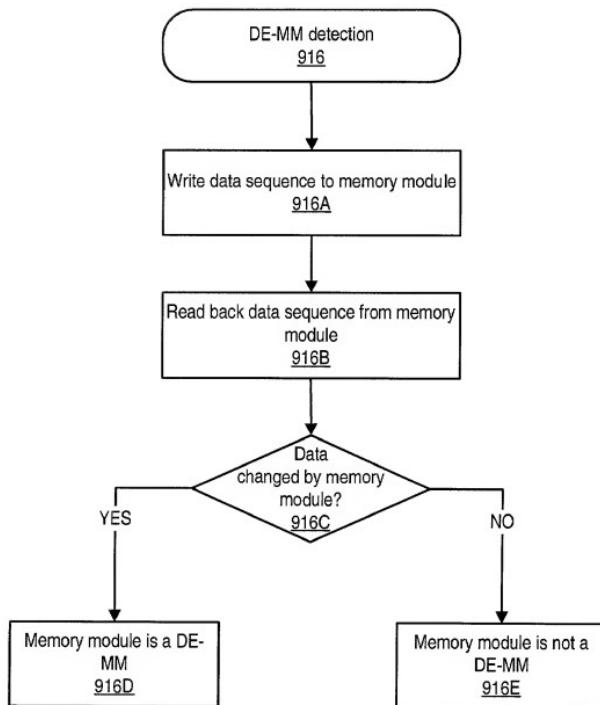


Figure 8

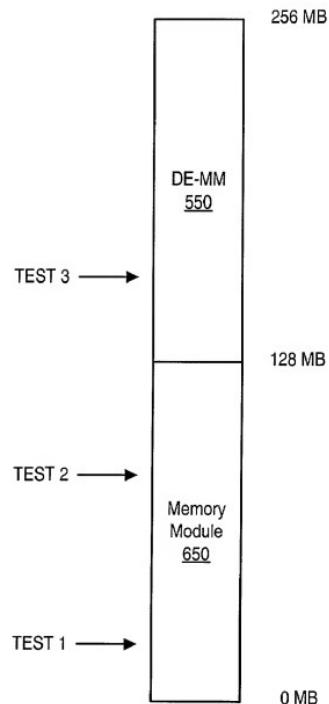


Figure 9

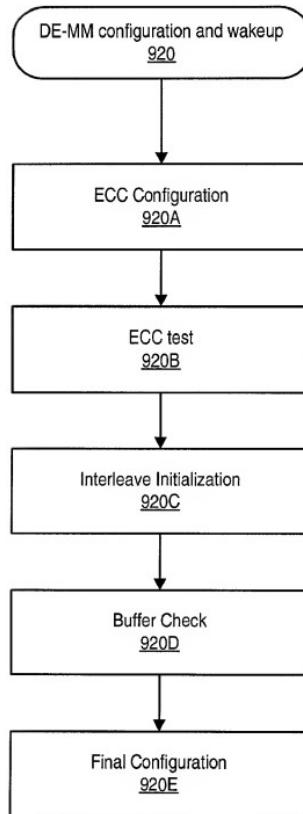


Figure 10

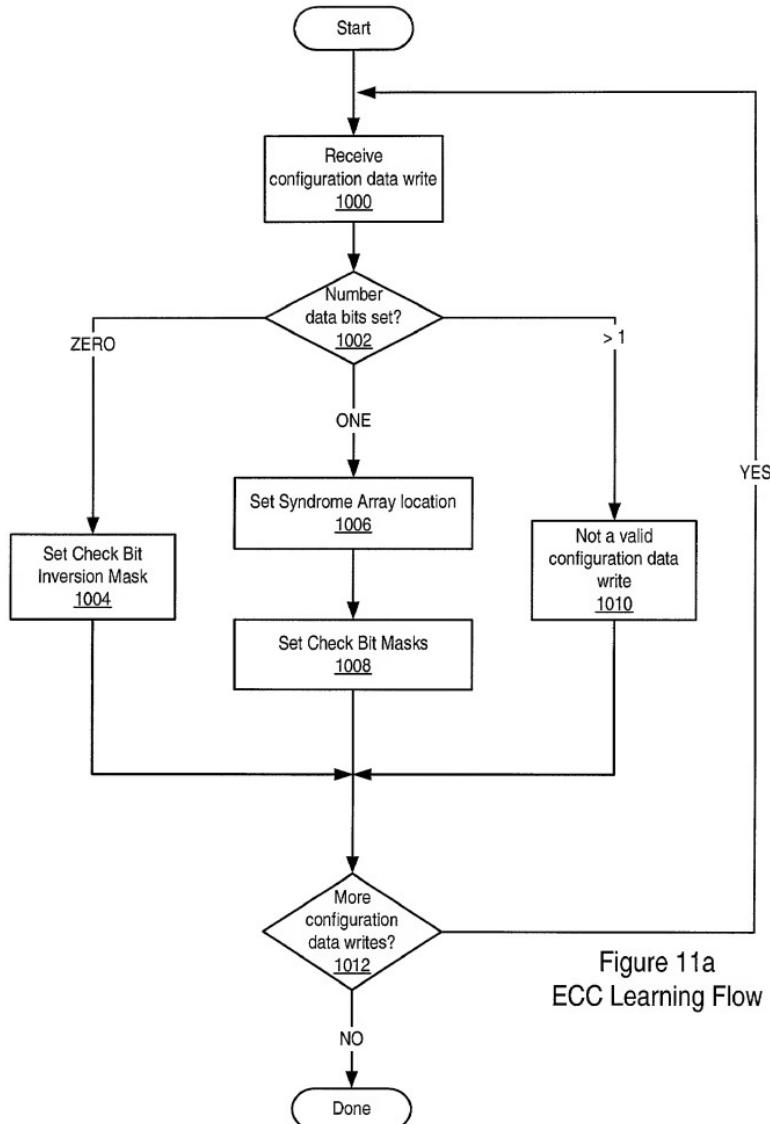


Figure 11a
ECC Learning Flow

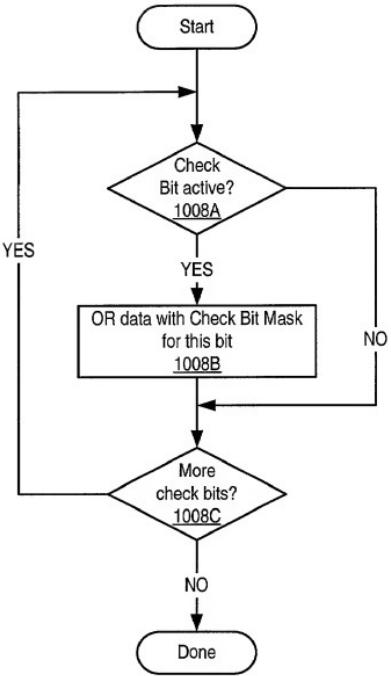


Figure 11b
Learning Check Bit Masks

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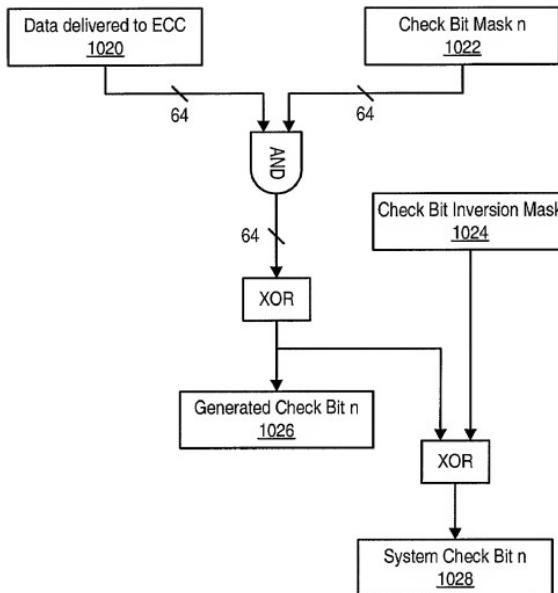


Figure 12
Check Bit Generation

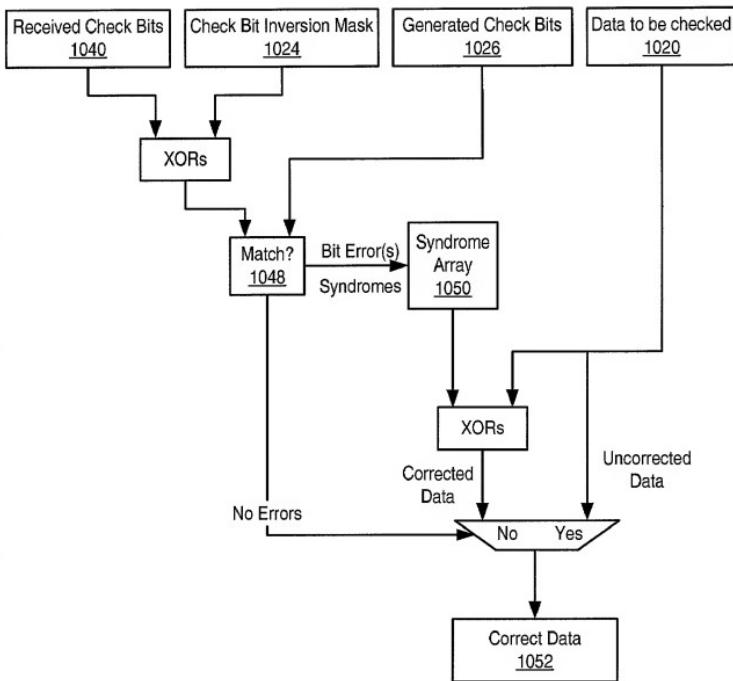


Figure 13
Data Checking and Correction

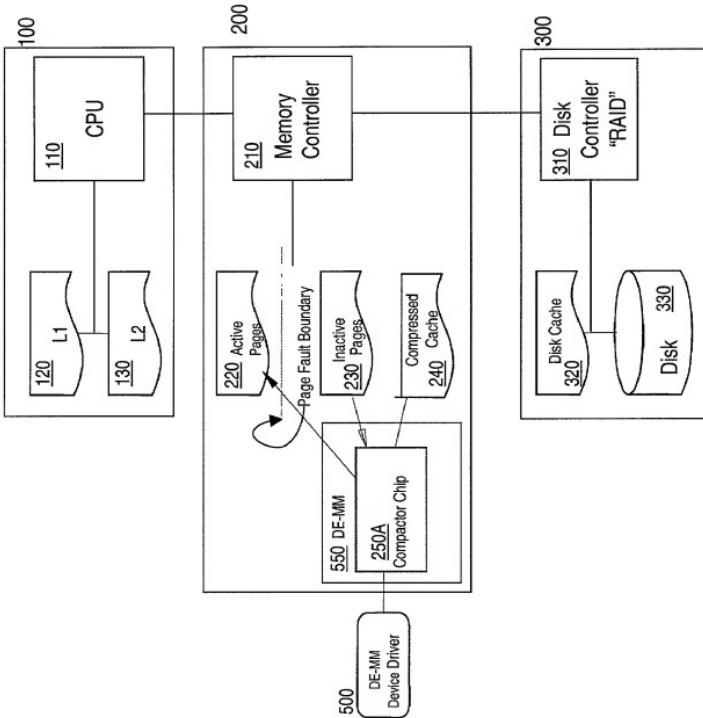


Figure 14

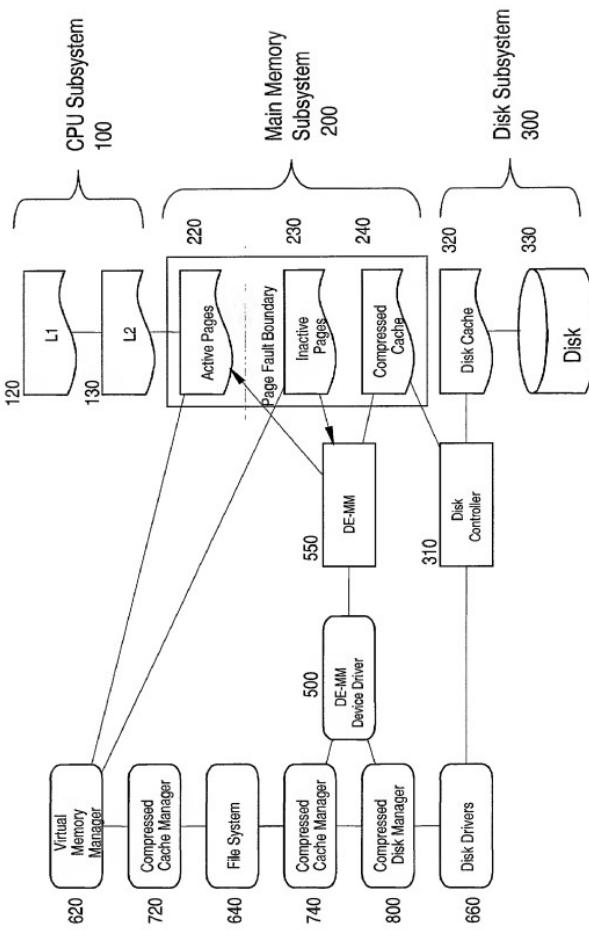


Figure 15